Dynamic-Space to Device to Exa-Scale

A three-companion-paper program for physics foundations, collective-gap switching, and 0.1 V / 100 GHz exa-scale compute fabrics

MIT presentation draft

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- Companion papers:
- 1. Dynamic-Space foundations
- 2. Super-steep collective-gap device
- 3. JSSC exa-scale GALS architecture

Three papers, one research arc

Each paper answers a different question: why this physics, how the device switches, and what system it enables.

Paper I

DS foundations

- Amplitude–phase field language
- Propagation vs. confinement
- Light bending and perihelion as DS propagation effects

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Paper II

Device physics

- Collective-gap transistor concept
- Sub-thermionic slope from gap softening
- Compact current model + parasitics

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Paper III

JSSC roadmap

- 0.1 V, 100 GHz local tiles
- GALS synchronization and short wires
- 100k × 100 stack exa-scale scaling

The trilogy is strongest because the papers are complementary rather than repetitive.

Paper I — Dynamic-Space foundations

Foundational physics paper: a common amplitude–phase language for radiation, matter, and weak-field gravity.

Core DS state

$$\Psi(\mathbf{x},t) = R(\mathbf{x},t)e^{i\phi(\mathbf{x},t)}$$

- **R^2** as local energy-density amplitude

∇ϕ
 as local momentum / propagation structure
Photons
 as propagating modes; matter as confined nonlinear modes
Gravity
 as amplitude–phase background deformation

Why it matters for the trilogy

DS is not the device paper itself; it supplies the unifying ontology that makes “collective-state switching” and “background-guided propagation” part of one framework.

Paper II — Super-steep collective-gap device

Device paper: a transistor concept where the gate tunes a collective transport gap rather than only a thermionic barrier.

Compact switching model

$$\Delta(V_G) \approx \Delta_0 \left[1 - \frac{\alpha(V_G - V_T)}{\nu_c}\right]$$

$$I_D = I_0 \exp\left(-\frac{\Delta(V_G)}{kT}\right)$$

$$S = \left(\frac{kT}{\Delta_0}\right)\left(\frac{\nu_c}{\alpha}\right) \ln 10$$

Design levers

- Large Δ_0 / kT
- Sharp gate coupling α / vc
- Low contact resistance and suppressed leakage
- Cryogenic operation where collective gaps dominate

Key contribution: a physically explicit non-Boltzmann switching mechanism that can be compact-modeled and benchmarked.

Paper III — JSSC roadmap to exa-scale

System paper: 0.1 V / 100 GHz tile-local operation, GALS synchronization, and 3D locality-preserving parallelism.

Critical equations

$$P_{dyn} \propto CV^2 f$$

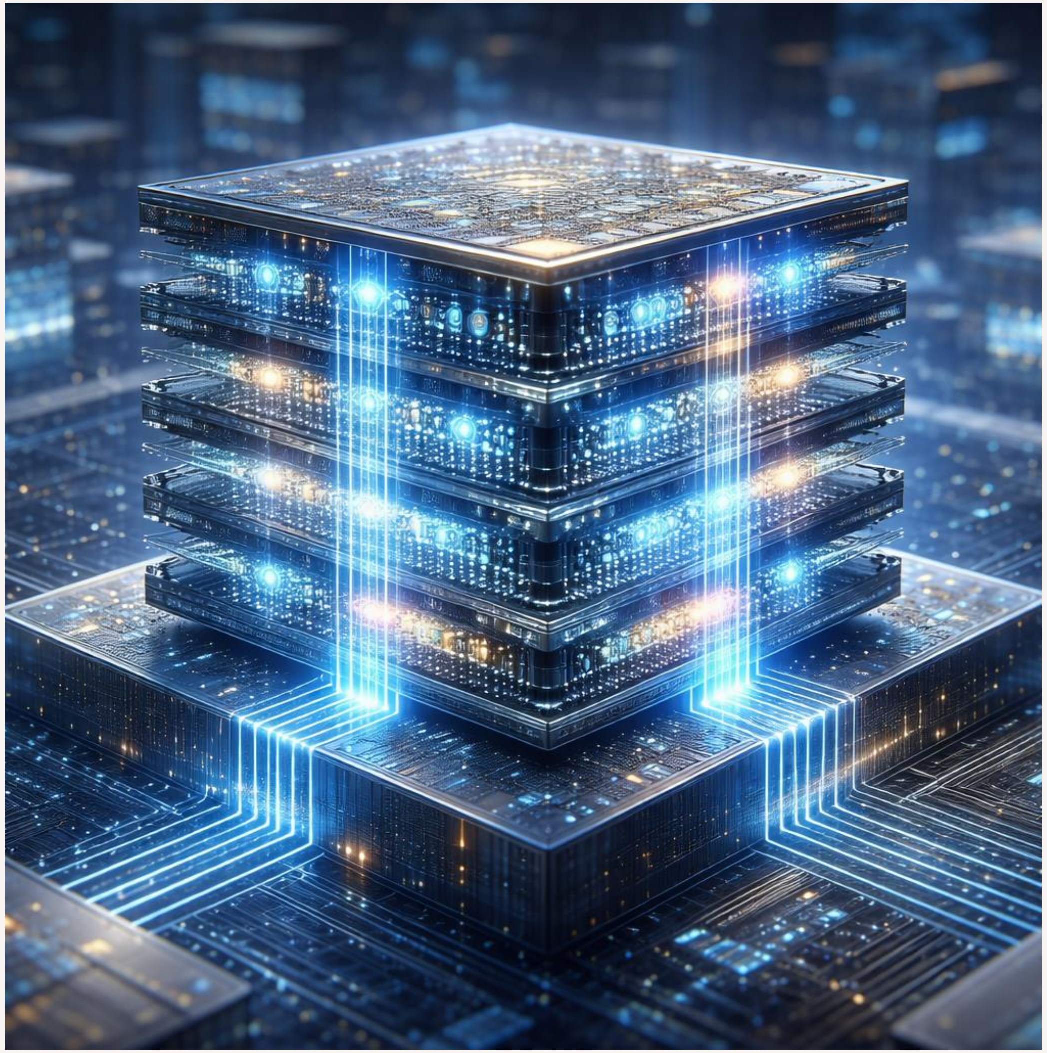
$$f_T = \frac{g_m}{2\pi C_{gg}}$$

$$\tau_{gate} \approx \frac{C_{eff} V_{DD}}{I_{on}}$$

Architecture implications

- 100 GHz is plausible only for tile-local timing
- Global synchronization must give way to GALS
- GPU-like fabrics fit better than monolithic CPUs
- Short wires and 3D locality are as important as steep slope

This paper turns the device into an architecture target.



The exa-scale anchor equation

The arithmetic works. The engineering challenge is power density, current drive, interconnect, and thermal extraction.

$$100\ \mathrm{GHz} \times 100{,}000\ \mathrm{processors/layer} \times 100\ \mathrm{layers} = 10^{18}\ \mathrm{processorext{-}cycles/s}$$

What is immediate

- One useful op per cycle already reaches exa-scale baseline
- GPU-style tiles maximize locality and reuse
- 0.1 V helps counter the 100× frequency increase

What is hard

- Externally usable current at low voltage
- Wire delay once communication escapes the tile
- 3D thermal density and vertical integration

Why the trilogy matters

- DS explains the conceptual language
- Device paper makes the switching explicit
- JSSC paper makes the scaling testable

Why this is a credible MIT-style research program

Not one giant claim—three linked papers with distinct risk profiles, milestones, and validation paths.

Immediate validation tasks

- Extract compact-model parameters from candidate collective-gap platforms
- Build Verilog-A / SPICE model and validate inverter + ring oscillator
- Quantify contact resistance, leakage floor, and switching broadening
- Prototype tile-local timing and GALS synchronization overhead

Program payoff

A rare complete arc: foundational field theory → explicit switching device → exa-scale architecture target.

One coherent research thesis

Physics → Device → System

$$\mathrm{DS} \to \text{collective-gap transistor} \to 0.1\ \mathrm{V}\ /\ 100\ \mathrm{GHz}\ \text{exa-scale fabric}$$

The scientific value is not only the destination. It is the consistency of the path.

Ask: evaluate this as a companion-paper program with one shared spine and three publication targets.