A Collective-Channel Transistor Concept Inspired by Quantum Hall Edge Transport for Ultra-Low-Voltage Logic

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***Abstract*—A collective-channel transistor concept is proposed in which the dominant drain current is carried not by a conventional inversion layer, but by a gate-controlled coherent transport path inspired by quantum Hall edge transport. A compact phenomenological model is introduced in the form $I_D = I_{\mathrm{leak}} + C(V_G)\, I_{\mathrm{path}}$, where $C(V_G)$ is interpreted as a coherent-channel availability factor rather than a classical inversion-charge factor. Illustrative transfer and output characteristics show how steep apparent turn-on can arise from channel activation rather than conventional thermionic modulation. The most credible first validation is identified as a cryogenic quantum Hall testbed under a superconducting perpendicular magnetic field, followed by on-chip magnetic-texture-assisted devices and, ultimately, room-temperature topological or effective-field implementations. The proposed framework offers a compact device perspective for ultra-low-voltage logic beyond conventional MOSFET scaling.**

***Index Terms*—Quantum Hall effect, fractional quantum Hall effect, topological transistor, ultra-low-voltage logic, compact model, quantum point contact, edge channel, steep-slope device.**

I. Introduction

Conventional CMOS scaling increasingly faces severe electrostatic, transport, and power-density constraints. This motivates transistor concepts that switch by controlling a dominant transport path rather than by relying solely on thermionic barrier modulation. Quantum Hall and related topological transport systems provide a particularly instructive example: current is concentrated in edge channels while the bulk can remain strongly suppressed, and split-gate quantum point contacts (QPCs) can sharply modulate edge-channel transmission by changing local confinement or inter-edge coupling [1], [2].

This letter proposes a *collective-channel transistor* abstraction motivated by that physics. The central idea is that the gate determines whether a dominant coherent or quasi-topological transport path exists between source and drain. In contrast to a conventional MOSFET, the gate is not interpreted primarily as an inversion-charge generator. Instead, it acts as a selector of channel availability, transmission, or percolation. The long-term target is an ultra-low-voltage logic device in which the ON current is dominated by a sharply activated collective path.

The present work does not claim a finalized room-temperature implementation. Rather, it introduces the device concept, a compact phenomenological model, illustrative current–voltage characteristics, and a three-stage validation roadmap spanning (i) a cryogenic quantum Hall proof-of-principle, (ii) on-chip magnetic-texture-assisted channel shaping, and (iii) practical room-temperature topological or effective-field platforms.

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II. Collective-Channel Device Concept

Fig. 1 conceptually contrasts a conventional MOSFET with the proposed collective-channel transistor. In a MOSFET, the gate induces inversion charge and current increases by lowering the source-to-channel barrier and populating a diffusive channel. In the proposed device, the gate instead controls the existence or transmission of a dominant coherent path.

The inspiration comes from quantum Hall transport. A perpendicular magnetic field creates a quantized transport manifold consisting of Landau-quantized bulk states and edge channels. At selected filling factors, the bulk becomes effectively insulating or incompressible, while transport is carried primarily by edge states. In a practical switching element, the gate is not intended to dynamically modulate the magnetic field. Rather, a static quantizing environment establishes the channel manifold, while the gate modifies local carrier density, confinement geometry, edge-channel separation, or tunneling probability. In this sense, the magnetic field (or its effective topological analog) creates the channel physics, while the gate determines whether a coherent source-to-drain path exists.

III. Compact Phenomenological Model

We introduce the compact current model

$$I_D = I_{\mathrm{leak}}(V_G, V_D) + C(V_G, V_D)\, I_{\mathrm{path}}(V_G, V_D), \quad (1)$$

where I_{leak} is the residual leakage or nonideal branch, I_{path} is the current available through the dominant coherent path, and $C \in [0, 1]$ is a channel-availability factor.

Unlike a MOSFET compact model, C is *not* interpreted as inversion-layer formation. Instead, C captures the gate-controlled effectiveness of coherent-path formation, such as edge-channel transmission through a QPC-like constriction, local filling-factor alignment, inter-edge tunneling suppression, or collective-path percolation in an effective topological channel network.

A convenient illustrative form is

$$C(V_G) = \frac{1}{1 + \exp\left[-\dfrac{V_G - V_T^*}{V_S^*}\right]}, \quad (2)$$

where V_T^* is an effective channel-activation threshold and V_S^* is a channel-activation sharpness parameter. For a Stage-1

quantum Hall or QPC-like proof-of-principle, the path current may be viewed as

$$I_{\mathrm{path}} \approx G_{\mathrm{edge}}\, T(V_G)\, V_D, \tag{3}$$

where G_{edge} is a quantized or near-quantized conductance scale and $T(V_G)$ is a gate-controlled transmission coefficient.

IV. Illustrative Characteristics

Fig. 2 shows illustrative transfer and output characteristics generated from the model in (1)–(3). These curves should be interpreted as *phenomenological proof-of-principle characteristics*, not as calibrated room-temperature CMOS data. The most realistic physical interpretation is a Stage-1 cryogenic quantized-transport platform, such as a split-gated quantum Hall constriction or related mesoscopic edge-channel device under a strong perpendicular magnetic field.

The key objective of such a first demonstration is not final drive current, but rather the observation of (i) a dominant gate-controlled coherent path, (ii) sharp transfer behavior associated with path activation, (iii) suppressed leakage or bulk conduction, and (iv) reproducibility of a compact model of the form in (1). This distinction is essential: the initial demonstration validates the switching principle, while the eventual technology target seeks to transfer the same channel-activation mechanism into larger-gap, higher-temperature, and more scalable platforms.

V. Three-Stage Roadmap

Fig. 3 summarizes a practical three-stage development path.

A. Stage 1: Cryogenic Quantum Hall Proof-of-Principle

The first and most credible validation is a high-mobility two-dimensional channel (e.g., GaAs/AlGaAs or graphene/hBN) operated under cryogenic conditions in a perpendicular superconducting magnet. A split-gate QPC or Hall-bar constriction is used to modulate edge-channel transmission. In this phase, the external magnet is not part of the final product architecture; it is a scientific validation tool that establishes the quantized transport manifold and enables a clean test of gate-controlled collective-channel switching.

B. Stage 2: On-Chip Magnetic-Texture-Assisted Channel Control

The second stage replaces the bulky external field with localized magnetic bias or texture, such as patterned ferromagnetic or ferrimagnetic nanostructures, magnetic underlayers with strong stray-field gradients, or hybrid magnetic/electrostatic confinement. The objective is not necessarily to reproduce textbook fractional quantum Hall physics in full, but to preserve the functional principle of gate-controlled dominant-channel activation in a more localized device environment.

C. Stage 3: Practical Room-Temperature Collective-Channel Devices

The long-term target is a practical transistor platform in which a large effective transport gap and edge- or channel-dominant conduction arise without a large external magnetic field. Candidate routes include quantum anomalous Hall effect (QAHE) and Chern-insulating systems, magnetic topological materials, Berry-curvature-engineered channels, or collective resonant channels that emulate quantum-Hall-like path activation. In this stage, the proposed architecture becomes an ultra-low-voltage transistor concept rather than a mesoscopic physics demonstrator.

VI. Discussion

The proposed collective-channel abstraction is intentionally broader than a literal fractional quantum Hall transistor. Existing literature already demonstrates gate-controlled transmission of integer and fractional quantum Hall edge channels in split-gated QPC structures [1], [2]. Thus, the novelty claimed here is not the existence of gate control itself, but the recasting of that physics into a transistor-centric compact model and a scalable device roadmap.

From a circuit perspective, the proposed model suggests a class of devices whose apparent steepness is governed by channel-availability dynamics rather than solely by Boltzmann-limited barrier modulation. This does not automatically guarantee rigorous sub-$60\,\mathrm{mV/dec}$ behavior under conventional transistor metrology, but it motivates a distinct pathway to steep switching based on path selection, tunneling geometry, and collective-state alignment.

VII. Conclusion

A collective-channel transistor concept has been proposed in which the gate primarily controls the availability of a dominant coherent transport path rather than merely generating an inversion layer. Inspired by quantum Hall edge transport and gate-defined constrictions, the device is described by a compact phenomenological model $I_D = I_{\mathrm{leak}} + C\, I_{\mathrm{path}}$, where C is a coherent-channel availability factor. The present IV characteristics are best interpreted as proof-of-principle behavior for a cryogenic quantized-transport platform under a strong external magnetic field. A three-stage roadmap was outlined, spanning superconducting-magnet validation, on-chip magnetic-texture-assisted devices, and practical room-temperature topological or effective-field implementations. This framework offers a concise device-level path for exploring ultra-low-voltage logic beyond conventional CMOS scaling.

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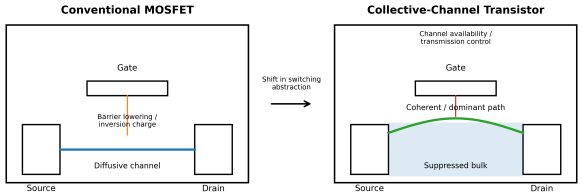

Fig. 1. Conceptual comparison between a conventional MOSFET and the proposed collective-channel transistor. In the latter, the gate primarily controls coherent-path availability rather than inversion-layer formation.

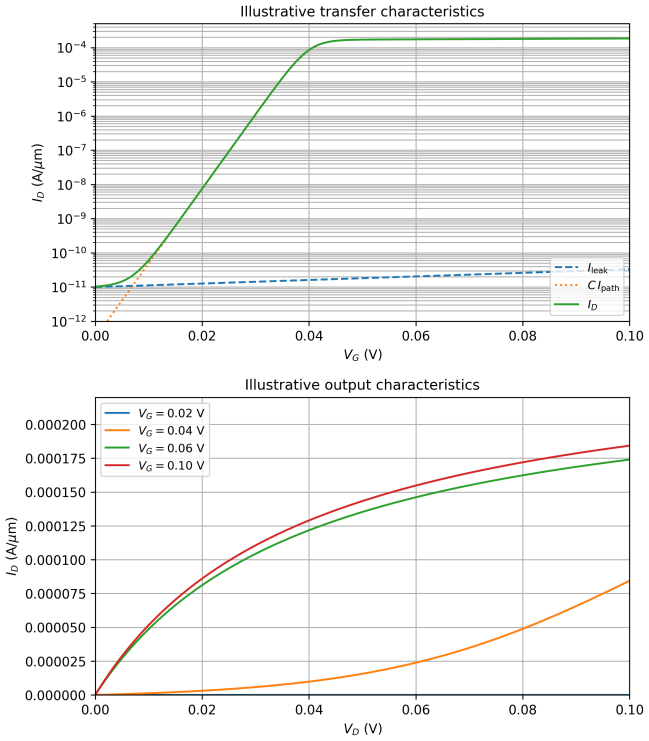

Fig. 2. Illustrative proof-of-principle transfer and output characteristics of the collective-channel transistor concept. These curves are phenomenological and are best interpreted as a Stage-1 cryogenic quantized-transport demonstration rather than calibrated room-temperature CMOS data.

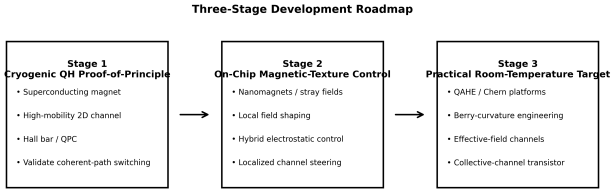

Fig. 3. Three-stage roadmap: (Stage 1) cryogenic quantum Hall proof-of-principle under a superconducting magnet, (Stage 2) on-chip magnetic-texture-assisted channel shaping, and (Stage 3) practical room-temperature collective-channel devices based on topological or effective-field platforms.

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